inconsistent with the terms of claim 21. That is, the diamond film layer 16 of figure 7 is not "between and over" any combination of transistor gates 14 and vias 18. Nor would the rejection meet the terms of claim 21 if the examiner read the claimed "second insulative layer" upon Jeng's diamond film layer 16 shown in figures 3 and 4. Further it would be improper to attempt to read the claim "second insulative layer" upon both of the referenced layers 16 because these are distinct and different layers.

In addition to the above, it is improper to reinterpret a transistor gate or a via as one of applicants' interconnect members. See page 5, line 5-6 of the application. Finally, an inconsistency exists between the examiner's characterization of layer 12 as insulative and Jeng's statement that layer 12 is a semiconductor substrate. See col. 3, lines 33-35.

With regard to claim 23, it is not understood how the examiner can possibly bring this rejection forward when the examiner reads applicants' "second insulative layer" on Jeng's diamond film layer 16. Further, it is noted that the examiner cannot substitute the silicon dioxide referenced at col.3, lines 45-55 for layer 16 because the examiner has already read applicant's "first insulative layer" on Jeng's layer 12.

The cited deficiencies render rejection of all other claims depending from claim 22 improper as well.

Claims 27 and 31 are amended to fully distinguish over the art of record. None of the art alone or in combination teaches or suggests the ordered sequence of steps which applicants have now made more clear. Further, each of

the dependent claims further distinguishes over the prior art. By way of example, note that claim 29 requires in part: "one or more of the conductor lines masking other portions of the first insulative material ..." This feature is not taught or suggested by any of the art of record.

For all of the above reasons the rejections are improper and it is submitted that the claims are allowable over the art of record. Applicant has fully addressed the examiner's rejections and believes the application is now in condition for allowance. If the examiner finds any additional deficiencies it is requested that the examiner telephone the undersigned in order to address any remaining concerns.

Respectfully submitted,

By Ferdinand M. Romano

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407-371-3250

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Version With Markings to Show Changes Made

1. Kindly write the title of the application as follows:

Integration of Low K Dielectric Material in Semiconductor Circuit Structures.

2. Kindly write claim 27 as follows:

A method for fabricating an integrated circuit structure comprising:

forming multiple levels of conductor lines over one another with some of the levels separated from one another by a layer of first insulative material;

then replacing portions of the first insulative material with a second insulative material having a dielectric constant lower than that of the first insulative material.

3. Kindly write claim 31 as follows:

A method for fabricating an integrated circuit having interconnect members formed over a semiconductor surface, comprising:

providing a first insulator material between interconnect members;

then replacing portions of the first insulator material with a dielectric material having a lower dielectric constant than the first insulator material.